REMARKS

This Application has been carefully reviewed in light of the Advisory Action mailed June 3, 2005. In order to advance prosecution of this Application, Claims 1, 11, and 16 have been amended. Applicant respectfully requests reconsideration and favorable action in this case.

The Examiner issued a Final Action on March 23, 2005. Applicant submitted a Response to Examiner's Final Action on May 19, 2005. The Examiner issued an Advisory Action on June 3, 2005 stating that the Response to Examiner's Final Action would not be entered because it raised new issues requiring further searching and consideration. Applicant respectfully requests continued examination of this Application so that the Response to Examiner's Final Action be entered and considered by the Examiner pursuant to this Request for Continued Examination. For the convenience of the Examiner, the amendments made to the claims in the Response to Examiner's Final Action and the accompanying comments are repeated herein.

Claims 1, 2, and 4-20 stand rejected under 35 U.S.C. §102(b) as being anticipated by Kabemoto, et al. Independent Claim 1 recites ". . . each processor including an integrated memory operable to provide/receive/store data, each processor including a central processing unit with an integrated memory controller operable to control access to the integrated memory and an integrated memory directory operable to maintain a plurality of memory references to data within the integrated memory . . ." By contrast, the Kabemoto, et al. patent shows processor and cache units separate from each other and a separate memory control module. Moreover, a directory memory is disclosed as being separate and apart from the processor. The Examiner has referred to processor element 14-1 of the

Kabemoto, et al. patent in stating that each component of the claimed invention is found therein but has not shown how the processor 16-1 itself includes each component of the processor of the claimed invention. The processor element 14-1 of the Kabemoto, et al. patent includes a processor 16-1, a cache unit 18-1, and a snoop unit 20-1. The Examiner shows that the processor 16-1 of the Kabemoto, et al. patent includes a memory 36 and 38 but readily admits that a memory controller 35 and a memory directory 40 of the Kabemoto, et al. patent are not included in its processor 16-1 by showing that the memory controller 35 and the memory directory 40 are in the cache unit 18-1 which is separate and apart from the processor 16-1. As a result, the processor of the Kabemoto, et al. patent does not include the resources and functionality of the processor in the claimed invention. Thus, the Kabemoto, et al. patent does not have a processor that includes an integrated memory and a central processing unit with an integrated memory controller and an integrated memory directory as provided by the claimed invention. Therefore, Applicant respectfully submits that Claims 1, 2, and 4-20 are not anticipated by the Kabemoto, et al. patent.

Claims 1, 2, 5, 6, 9-11, and 13-17 stand rejected under 35 U.S.C. §102(e) as being anticipated by Chase, et al. Independent Claim 1 recites ". . . each processor including an integrated memory operable to provide/receive/store data, each processor including a central processing unit with an integrated memory controller operable to control access to the integrated memory and an integrated memory directory operable to maintain a plurality of memory references to data within the integrated memory . . ." By contrast, the station 12 of the Chase, et al. patent equated by the Examiner as the claimed processor shows a processor 18 and a storage 21 with a

cache 20 separate and apart from its processor 18. Thus, the storage 21 and cache 20 of the Chase, et al. patent are not integrated within its processor 18 as would be required by the claimed invention. Therefore, the Examiner has failed to show how the Chase, et al. patent has a processor with an integrated memory when the Chase, et al. patent specifically shows a separate processor 18 and a separate storage 20 that is not included within the processor 18.

The Chase, et al. patent expressly discloses a cache directory 16 in a directory server 17 that is separate and apart from station 12 and its processor 18 and storage 21. The Chase, et al. patent clearly discloses the use of a cache directory 16 in a server 17 separate and remote from any of its stations 12 for use with cache 20 within station 12. The Chase, et al. patent clearly teaches away from any use of a directory within its station 12 let alone being integrated with its processor 18 as would be required by the claimed invention. Thus, the memory directory of the Chase, et al, patent is not integrated in a processor as required by the claimed invention. In fact, the memory directory 16 is disclosed in the Chase, et al. patent as also being separate from a processor 18 within its directory server 17.

Further, the Chase, et al. patent provides no mention of a memory controller within station 12 or processor 18 let alone any integration of a memory controller within its processor 18. All of the portions of the Chase, et al. patent cited by the Examiner clearly show a memory controller being separate and apart from its corresponding processor. Thus, not only does the Chase, et al. patent fail to show a local memory and memory controller integrated within a processor, there is also no support in the Chase, et al. patent for a memory directory integrated in the processor along with a

local memory and memory controller as required by the claimed invention.

Applicant's specification specifically shows that the term 'integrated' defines these elements as being within a single device, the processor. The Chase, et al. patent teaches away from this integration by having all of the claimed elements in separate devices. The processor of the Chase, et al. patent does not include the resources and functionality of the processor in the claimed invention. As a result, the Examiner has not provided any teaching within the Chase, et al. patent to support the rejection of the claims. Thus, without a reference that discloses each and every limitation or a reference combinable with the Chase, et al. patent to support a rejection, the Chase, et al. patent by itself is insufficient to support a rejection of the claimed invention. Therefore, Applicant respectfully submits that Claims 1, 5, and 7-10 are not anticipated by the Chase, et al. patent.

Claims 3, 10, 18, and 20 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Chase, et al. Claim 1, from which Claims 3 and 10 depend, and Independent Claim 16, from which Claims 18 and 20 depend, have been shown above to be patentably distinct from the Chase, et al. patent. Therefore, Applicant respectfully submits that Claims 3, 10, 18, and 20 are patentably distinct from the Chase, et al. patent.

Claim 3 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Kabemoto, et al. Claim 1, from which Claim 3 depends, has been shown above to be patentably distinct from the Kabemoto, et al. patent. Therefore, Applicant respectfully submits that Claim 3 is patentably distinct from the Kabemoto, et al. patent.

Attached herewith is a check in an amount of $790.00 made payable to the "Commissioner of Patents and Trademarks" to satisfy the request for continued examination fee of 37 C.F.R. §1.17(e).

CONCLUSION

Applicant has now made an earnest attempt to place this case in condition for allowance. For the foregoing reasons, and for other reasons clearly apparent, Applicant respectfully requests full allowance of all pending claims.

The Commissioner is hereby authorized to charge any fees or credit any overpayments to Deposit Account No. 02-0384 of BAKER BOTTS L.L.P.

Respectfully submitted,
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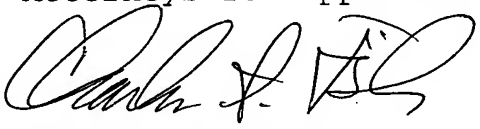

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